35. ITG / GMM / GI-Workshop
Workshop Test Methods and Reliability of Circuits and Systems
26.2. to 28.2.2023, Erfurt

Program

Sunday, 26th February 2023

17:00 - 19:30	Registration
18:00 - 20:00	Dinner
20:00 - 21:30	Public meeting of the GI/GMM/ITG-section "Testmethoden und Zuverlässigkeit von Schaltungen und Systemen"

Monday, 27th February 2023

8:00 - 8:30	Registration
8:30 - 9:00	Opening

Keynote I — Chair: Matthias Sauer

9:00 – 10:00

DfT for achieving 0 DPPB, are we there yet?
Tom Waayers
Technical Director DfT bei NXP

10:00 – 10:30 Coffee break

Session 1: Fault tolerance/Life cycle test — Chair: Leticia Poehls

10:30 – 12:00

Aging-Aware Task Deployment of Heterogeneous Multicore System
Ing-Chao Lin, Jie-Shih Wang
National Cheng Kung University, Taiwan
Yu-Guang Chen
National Central University, Taiwan
Ulf Schlichtmann
Technische Universität München

Der TETRISC SoC - Ein resilientes Quad-Core System auf Pulpissimo-Basis
Markus Ulbricht, Junchao Chen, Li Lu
IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)
Milos Krstic
Universität Potsdam und IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)
Wolfgang Müller
Universität Paderborn

Messumgebung für Lebensdauertests basierend auf dem Konzept der universellen Test-Chips (UTC)
Bjoern Bieske, Ingo Gryl
IMMS GmbH Ilmenau
Pierre Wenke, Martin Jäger, Xiao Liu, Jörg Steinecke
X-FAB Semiconductor Foundries GmbH Erfurt

12:00 – 13:00 Lunch break

Session 2: Verification and Modeling — Chair: Sebastian Huhn

13:00 – 14:30

Characterization and Modeling of Single Event Transient Propagation through Standard Logic Cells
Marko Andjelkovic
IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)
Milos Krstic
Universität Potsdam und IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)

New Directions for Equivalence Checking of System-Level and SPICE-Level Models of Linear Circuits
Kemal Caglar Coskun
University of Bremen
Muhammad Hassan, Rolf Drechsler
DFKI GmbH and University of Bremen

Verification Bio-Electronic Systems
Joseline Heuer, Rene Krenz-Baath
Hochschule Hamm-Lippstadt
Roman Obermaisser
University of Siegen

14:30 – 15:00 Coffee break

Session 3: Safety and Security — Chair: Ilia Polian

15:00 – 16:00

Towards: Threat Modeling in System Design
Bernhard J. Berger, Görschwin Fey
Hamburg University of Technology

DoCNeL: Detection of Crucial Neurons Guided by Layer-wise Relevance Propagation
Fin H. Bahnsen, Bernhard J. Berger, Görschwin Fey
Hamburg University of Technology

16:30 – 22:30 Social Event

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Tuesday, 28th February 2023

Keynote II

Chair: Jürgen Alt

8:30 – 9:30

The EU Chips Act and US export controls – Why governments now care about chips

Jan-Peter Kleinhans
Head of Technology and Geopolitics at Stiftung Neue Verantwortung, Berlin, Germany

Session 4: Short presentations

Chair: Görschwin Fey

9:30 – 10:00

Verbesserte Analyse des Lokatorpolynoms bei 2-Bit-Fehler-korrigierenden BCH-Codes

Christian Min Hansch
Universität Potsdam

An Approach For Runtime Reconfigurability in Application-Specific CNN Accelerators

Rizwan Tariq Syed, Marko Andjelkovic, Markus Ulbricht
IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)
Milos Krstic
University of Potsdam und IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)

Poster session with pitches and coffee break

Chair: Marcel Merten

10:00 – 11:15

Enabling Silicon Lifecycle Management with programmable logic in SoC DfT-Infrastructure

Sergej Meschkov, Dennis R. E. Gnad, Jonas Krautter, Mehdi B. Tahoori
Karlsruhe Institute of Technology (KIT)

Multi-node Virtual Prototype simulator for IoT security application testing

Ernesto Cristopher Villegas Castillo, Christian Sauer
Cadence Design Systems, Munich, Germany

On Cryptography Effects on Interconnect Reliability

Abdulkarim Ghazal, Somayeh Sadeghi-Kohan, Jan Dennis Reimer, Sybille Hellebrand
University of Paderborn, Germany

Design and Validation of Custom Stacked-PCB Interposers for Acquisition of High-Speed Signals

David Riehl, Timo Oster, Mohammad Zidan, Klaus Hofmann
Technische Universität Darmstadt, Germany

Multiple Bit Upset-Tolerant EDAC Approach for Robust Embedded Memory Systems Design

Roger C. Goerl
Catholic University - PUCRS, Brazil
Paulo R. C. Villa
Federal University of Santa Catarina - UFSC, Brazil
Letícia Poehls
Aachen University, Germany
Fabian Vargas
IHP - Microelectronics, Germany

Session 5: Test and DfT

Chair: Stephan Eggersglüß

11:15 – 12:45

SPAREST - Smart Part Average Testing

Albert-Jan Knevels, Illia Khvastunov, Kim Van der Elstraeten, Kristof Coddens, Matthieu Van Malleghem
Melexis Technologies NV, Melexis NV

Remote Configuration Methodology for IEEE 1687 Scan Networks

Payam Habiby
University of Bremen, Germany
Sebastian Huhn, Rolf Drechsler
DFKI GmbH and University of Bremen, Germany

In-situ Trimming and Calibration System for Test Optimization

Myriam Massei, Ludwig Cron
Melexis NV/BO France
Hans Beauprez
Melexis Technologies NV
Emmanuel Riou
Melexis NV/BO France
Martin Zaspel, Andreas Ott
Melexis GmbH

12:45 – 13:00 Closing

13:00 – 14:00 Lunch

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